

Applicants are hereby amending FIG. 3 to make it consistent with the specification (col. 5, lines 60-61). A redlined copy of FIG. 3 is enclosed herewith. The Examiner is asked to approve this change to FIG. 3.

The Examiner's Form PTO-892 accompanying the Office Action cites all of the references cited in the parent issued patent. However, the Examiner fails to cite U.S. Patent No. 5,010,325 and European Patent No. 0240749. These references were cited as Items A18 and B3, respectively, in Applicants' Invention Disclosure Statement dated April 15, 2002. Additionally, Item C, page 4, of the Form PTO-892, incorrectly cites U.S. Patent No. 4,638,534 as a reference. The correct reference should be U.S. Patent No. 4,683,534 (See Item A33 in Applicants' IDS, dated 4/15/02).

The Examiner rejected claims 1-30 under 35 U.S.C. § 251, as being defective based on Applicants' failure to identify at least one error being relied upon as the basis for reissue. Applicants' have submitted with this response Supplemental Declarations correcting this deficiency.

The Examiner has requested Applicants to offer to surrender the original patent. Applicants will surrender the original patent when the Examiner has indicated that the application is in a condition for allowance.

In paragraph 1 of the Office Action, the Examiner rejected claims 23-30 under 35 U.S.C. § 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the original patent. Specifically, the Examiner identified three limitations (A), (B) and (C) that were omitted from claims 23, 26, and 28, and which formed the basis for the Examiner's rejections. Applicants have amended claims 23, 26 and 28 to include the limitations (A) and (B). Applicants traverse the Examiner's rejections of claims 23, 26 and 28 under 35 U.S.C. § 251, for allegedly omitting a limitation identified by the Examiner as limitation (C).

The Examiner identified limitation (C) as "means for switching the second clock to terminal used by the first clock; said means for switching the second clock to the terminals used by the first clock includes a multiplexer," as being the omitted limitation. Applicants traverse this rejection.

Claims 23, 26 and 28 each expressly recite a “multiplexer” element for switching between first and second clock signals.

Claim 23 recites:

“...a multiplexer having inputs coupled to the first clock signal and the second clock signal, and an output coupled to the buffer, the multiplexer supplying the first clock signal to the buffer to clock data from the source component to the buffer via the data path in the absence of a gate signal from the destination component, the multiplexer supplying the second clock signal to the buffer to clock data from the buffer to the destination component via the data path in response to the gate signal from the destination component without clocking other data from the source component to the buffer via the data path...” (Emphasis added).

Claims 26 recites:

“...supplying the first and second clock signals to the buffer via a multiplexer having a plurality of inputs and an output coupled to the buffer, the inputs for receiving the first and second clock signals and a valid signal from the second component, the multiplexer supplying the second clock signal to the buffer in response to the valid signal...” (Emphasis added).

Claim 28 recites:

“...a multiplexer having inputs coupled to the first clock signal and the second clock signal, and an output coupled to the buffer, the multiplexer supplying the first clock signal to the buffer to clock data from the source component to the buffer via the data path in the absence of a gate signal from the destination component, the multiplexer supplying the second clock signal to the buffer to clock data from the buffer to the destination component via the data path in response to the gate signal from the destination component without clocking other data from the source component to the buffer via the data path...” (Emphasis added).

Applicants submit that careful examination of claims 23, 26 and 28 against the file history of the original patent suggests that the limitation added via Examiner’s Amendment F is recited in claims 23, 26 and 28, as indicated above. In Interview Summary, Paper No. 18, the Examiner stated: “the prior art did not teach or suggest individually or in combination a multiplexor coupled to the first and second component, the multiplexer receiving a signal from

the second component for furnishing a second clock signal from the second clock to the buffer to transfer data to the second component." This limitation is clearly covered in claims 23, 26, and 28, as shown above. Indeed, the recitation of the "multiplexer" element in claims 23, 26 and 28 is arguably narrower than the Examiner's Amendment F, because it also describes the selection signal for the multiplexer (i.e., "valid" signal or "gate" signal). The selection signal determines which clock signal will be provided to the buffer in accordance with the normal operation of a multiplexer, as is well understood by those with ordinary skill in the art.

Applicants respectfully request the Examiner to withdraw her rejection under 35 U.S.C. § 251 based on the alleged omission of limitation (C) in claims 23, 26 and 28.

In paragraph 3 of the Office Action, the Examiner rejected claims 1-7 under U.S.C. § 112, second paragraph, as having insufficient antecedent basis in certain limitations of the claims. Applicants have amended claims 1-5 and 7 to provide proper antecedent basis.

Applicants submit that this application is now in condition for allowance. Reconsideration and allowance of this application is hereby solicited.

Respectfully submitted,
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Dated: _____

By: _____ /s/
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